Remarks

Claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-62 are pending. Claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 were rejected by the Office Action, but were amended, and claims 59-62 are new claims. The original claims are amended to place them in better format. New claims are added to give better coverage to the many embodiments of the invention disclosed in the present application.

Objection to the Specification

The Office Action objected to the specification. Although no grounds were given for the objection, the Office Action stated,

> The disclosure is objected to because of the following informalities:
> - page 10, line 12: Change "Refer to the diagram titled" to -- Refer to Figure 1 titled--
> - page 11, lines 11 and 17: Change "In the diagram," to -- In Figure 2,--
> - page 12, lines 9-10: Change "The diagram titled, " to -- Figure 3 titled --.
> - page 13, line 22: Change "Refer to the diagram, titled" to -- Refer to Figure 4 titled --.
> page 13, line 32: Change "The schematic diagram titled" to -- The schematic in Figure 5 titled—

The above amendment to the specification adapts the suggested changes, and therefore the objection has been obviated.

The Drawings

The Office Action objected to the drawings as failing to comply with 37 CFR 1.84(p)(4) because the reference character "m," was used to designate both a module in Machine A and a different module in Machine B. Accordingly the reference characters

of the modules in machine B have been relabeled with primes. A corresponding amendment to the specification was also made.

Additionally, the caption at the bottom of FIG. 1 was moved from the drawings to the specification, and the drawings are amended by replacing FIGs. 1-4 with a better version of the same drawings, which were labeled "Replacement Sheets" in compliance with 37 CFR 1.21(d).

Accordingly, the drawings should now be in compliance with 37 CFR 1.84(p)(4), and the objection should be withdrawn.

Statutory Subject Matter, 35 USC 101

The Office Action rejected claims 1, 2, 5, 6, 8-18, 21, 23-29, 31-32, and 34-58 under 35 U.S.C. 101 because the claimed invention was allegedly directed to non-statutory subject matter.

Hardware based claims

Regarding claims 1, 2, 8-12, 17, 18, 26, 35-38, and 47-58 independent claims 1 and 17, are amended to recite a "hardware computing machine," which includes "hardware active elements." The Office Action stated, "The 'computing machine' is not necessarily hardware-based...." However, via the above amendment claims 1, 2, 8-12 recite a hardware computing machine and claims 17, 18, 26, 21, 23, 26-29, 31, 32, 34-38, and 47-58 recite a method for making a hardware computing machine (claims 21, 23, 27-29, 31, 32, and 34 recite steps that relate to designing the Effector machine as part of a method for building the Effector machine). Therefore claims 1, 2, 8-12, 17, 18, 21, 23,

26-29, 31, 32, 34-38, and 47-58 are now hardware based. Consequently, the invention of claims 1, 2, 8-12, 17, 18, 26, 35-38, and 47-58 no longer fall into a "judicial exception," and therefore the remainder of the comments relating to Benson and judicial exceptions do not apply.

Useful tangible results

Claims 5, 6, 14-16, and 39-48 recite designing an Effector machine. An Effector machine is a form of a computer capable of performing the tasks that any computer can perform and as such designing an Effector machine is a useful tangible result. Additionally, as disclosed, every design for an Effector machine is also a design for a VLSI. Specifically, as stated at the top of page 13 of the specification,

> it is very difficult to write a computer program that could automate the design of these circuits, using piecewise linear analysis. This greatly increases the time and financial cost of designing these circuits. CGE does not require cleverness. One can treat the analog VLSI circuit as a black box. All you need to know is for a set of inputs $\{I_1, I_2, \ldots\}$, what set of corresponding outputs, $\{O_1, O_2, \ldots,\}$, are required of the analog VLSI circuit. Then execute CGE on the *(input, output)* set, $\{(I_1, O_1), (I_2, O_2), (I_3, O_3), \ldots\}$

Thus, in addition to a design of an Effector machine being a useful and tangible result because it is a design of a computing machine, claims 5, 6, 14-16, and 39-48 recite a useful tangible output by reciting a design for an Effector machine, because a design for an effector machine is also a design for a VLSI.

No pre-emption

The Office Action alleged that the claims 1, 2, 5, 6, 8-18, 21, 23-29, 31-32, and 34-58 are so broad sweeping that they pre-empt many well established fields, such as Bayesian networks and neural networks.

However, regarding claims 2, 6, 8-16, 18-21, 23-29, 31-32, and 34-46, and 49-58, there is no art rejection. If the claims pre-empt an entire well established field, then any reference (with an early enough date) describing a device from that field should be a reference under 35 USC 102. Thus, for the claims not rejected, the lack of existence of references that are anticipatory indicates that those claims are not so broad sweeping as alleged by the Office Action, indicating that the Office Action has not shown any pre-emption to exist and that no principle has been pre-empted.

Regarding claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58, the pre-emption rule forbids a claim from being so broad that it pre-empts a fundamental principle, such as $E = mc^2$, Boolean algebra, or the use of electromagnetic waves. However, contrary to the implications of the Office Action, no such fundamental principle is expressed in any of these claims. Specifically, claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 as now amended do not pre-empt all computers, do not pre-empt all neural networks, do not pre-empt all genetic algorithms, do not pre-empt all parallel computers, do not pre-empt all Bayesien networks, and do not even pre-empt all machines having effectors or other active elements. Even to meet the limitations of independent claims 1 and 17 (the broadest claims), the Effector machine needs to have a plurality of Effectors and an architecture that "determines" (e.g., "adjusts") the connections of the Effectors within the very same Effector machine, and therefore pre-emption is not an issue.

Utility under 35 USC 101 and 112, first paragraph

The Office Action rejected Claims 1-2, 5-6, 8-18, 21, 23-29, 31-32, and 34-58 under 35 U.S.C. 101, because the claimed invention is alleged not to have utility, and also rejected claims 1-2, 5-6. 8-18, 21, 23-29, 31-32, and 34-58. The Office Action alleged regarding 35 USC 101 "no use for the claims has been claimed or disclosed." The Office Action further alleged regarding 35 USC 112, first paragraph, "when Applicant has not in fact disclosed the practical application for the invention, as a matter of law there is no way Applicant could have disclosed how to practice the undisclosed practical application."

However, contrary to the assertions about, "no use ... disclosed in the specification," the specification (in the paragraph bridging pages 12 AND 13) states,

> CGE can also improve the design of analog VLSI circuits which are suitable for implementing Effector machines in hardware. One of Mead's primary methods of designing subthreshold analog circuits, [MEAD], is to use piece wise linear analysis to design nonlinear circuits. Piecewise linear analysis becomes mathematically intractable as the size of the circuit increases. Also, piecewise linear analysis of them requires a person to come up with clever techniques for predicting how the circuit will behave. In other words, it is very difficult to write a computer program that could automate the design of these circuits, using piecewise linear analysis. This greatly increases the time and financial cost of designing these circuits. CGE does not require cleverness. One can treat the analog VLSI circuit as a black box. All you need to know is for a set of inputs {I1,I2,...}, what set of corresponding outputs, {O1,O2,...,} , are required of the analog VLSI circuit. Then execute CGE on the (input, output) set, {(I1,O1), (I2,O2), (I3,O3),...}.

In other words, CGE, which is disclosed to be executed on an Effector machine can be used to design an analog VLSI circuit. Thus, the specification explains that one utility of an Effector machine is the design of VLSI circuits. To design a VLSI having a specific set of input output pairs one only needs implement a CGE program on an effector machine. The specification discloses designing Effector machines and using Effector

machines to design other Effector machines. Although the Effector machines claimed can be implemented on any type of hardware (not just a VLSI) that is capable of implementing the claimed collection of computational elements, every effector machine is also a design of a VLSI. Consequently, since every Effector machine is a design of a VLSI, the designing of Effector machines have utility as a method for desiging a VLSI and Effector machines are themselves tools that are used for designing VLSIs by designing other Effector machines. Thus, contrary the assertions of the Office Action, the specification asserts a specific, substantial and credible utility.

Additionally, at the top of page 2 the specification states,

> The Effector machine is a new kind of asynchronous computer. The Effector machine is not a digital computer. Its design has been influenced by Alan Turing's work in mathematics and computer science and Wilfred Rall's research in neurophysiology.

Similarly, in the abstract the specification states,

> An Effector machine is a new kind of computing machine. When implemented in hardware, the Effector machine can execute multiple instructions simultaneously because every one of its computing elements is active.

Thus, the Effector machine is disclosed to be a new type of computer, and has utility as a computer. Computers are ubiquitous in today's society, and are used as word processors in nearly every office in the United States and Europe and many households. Additionally, computers are used for search machines, picture processors, databases, analysis of data, and many other uses. Effector machines are disclosed as "a new type of computing machine," that can potentially out perform, and therefore are intended to replace, standard digital computers. Since Effector machines are intended to replace digital computers they have the same utilities as a digital computer.

Written Description Requirement under 35 USC 112, first paragraph

The Office Action rejected Claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The Office Action stated that

> Neither the claims nor the disclosure as a whole reasonably convey that Applicant had possession of a machine at the time of the invention, which when compared to today's digital computers, is capable of executing computations more than four orders of magnitude faster while consuming more than 5 orders of magnitude less power and producing less (sic.) much less heat.

However, claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58 do not recite, "when compared to today's digital computers, is capable of executing computations more than four orders of magnitude faster while consuming more than 5 orders of magnitude less power and producing less much less heat." Consequently, even if arguendo the applicant were not in possession of this technology, whether the Applicant was in possession of a fast low power Effector machine is not relevant to whether the Applicant was in possession of the invention of claims 1, 2, 5, 6, 8-18, 21, 23-29, 31, 32, and 34-58. The burden of proof is upon the Office Action, and Office Action has brought no proof to support that burden.

MPEP 2163, p. 2100-165, the bottom of the left column, states,

> The written description requirement has several policy objectives. "[T]he 'essential goal' of the description of the invention requirement is to clearly convey the information that an applicant has invented the subject matter which **is claimed**." *In re Barker*, 559 F.2d 588, 592 n.4, 194 USPQ 470, 473 n.4 (CCPA 1977) (emphasis added).

MPEP 2163, p. 2100-165, right column, also states,

> *>"The 'written description' requirement implements the principle that a patent must describe the technology that is sought to be patented; the requirement serves both to satisfy the inventor's obligation to disclose the technologic knowledge upon which the patent is based, and to demonstrate that the patentee was in

> possession of the invention that **is claimed**." *Capon v. Eshhar*, 418 F.3d 1349, 1357, 76 USPQ2d 1078, 1084 (Fed. Cir. 2005). (emphasis added).

In other words, in *In re Barker* and *Capon v. Eshhar* only the claimed subject matter needs to satisfy the written description requirement. Unclaimed subject matter does not affect whether the claims satisfy the written description requirement. Consequently the rejection under 35 USC 112, first paragraph, under the written description requirement is improper and should be withdrawn.

Additionally, MPEP 2107.1, p. 2100-24, states,

> An invention that is "inoperative" (i.e., it does not operate to produce the results claimed by the patent applicant) is not a "useful" invention in the meaning of the patent law. See, e.g., *Newman v. Quigg*, 877 F.2d 1575, 1581, 11 USPQ2d 1340, 1345 (Fed. Cir. 1989); *In re Harwood*, 390 F.2d 985, 989, 156 USPQ 673, 676 (CCPA 1968) ("An inoperative invention, of course, does not satisfy the requirement of 35 U.S.C. 101 that an invention be useful."). However, as the Federal Circuit has stated, "[t]o violate [35 U.S.C.] 101 the claimed device must be totally incapable of achieving a useful result." *Brooktree Corp. v. Advanced Micro Devices, Inc.*, 977 F.2d 1555, 1571, 24 USPQ2d 1401, 1412 (Fed. Cir. 1992) (emphasis added). See also *E.I. du Pont De Nemours and Co. v. Berkley and Co.*, 620 F.2d 1247, 1260 n.17, 205 USPQ 1, 10 n.17 (8th Cir. 1980) ("A small degree of utility is sufficient . . . The claimed invention must only be capable of performing some beneficial function . . . An invention does not lack utility merely because the particular embodiment disclosed in the patent lacks perfection or performs crudely . . . A commercially successful product is not required . . . Nor is it essential that the invention accomplish all its intended functions . . . or operate under all conditions . . . partial success being sufficient to demonstrate patentable utility . . . In short, the defense of non-utility cannot be sustained without proof of total incapacity." If an invention is only partially successful in achieving a useful result, a rejection of the claimed invention as a whole based on a lack of utility is not appropriate. See *In re Brana*, 51 F.3d 1560, 34 USPQ2d 1436 (Fed. Cir. 1995); *In re Gardner*, 475 F.2d 1389, 177 USPQ 396 (CCPA), *reh'g denied*, 480 F.2d 879 (CCPA 1973); *In re Marzocchi*, 439 F.2d 220, 169 USPQ 367 (CCPA 1971).

In other words, to be inoperative an invention must be "totally incapable of achieving a useful result (emphasis original)." Even if arguendo the Effector machine were not capable of performing computations at a rate of 4 to 5 time faster than a standard digital

computer while using less power, as stated in the specification, the Effector machine is still capable of performing computations at another rate and at another power level and therefore is not totally incapable of a useful result. Consequently, the Effector machine is operative.

Further, standard digital machines execute instructions sequentially. In contrast, the instructions of an Effector machine can be carried out in parallel. . Now the claims in the specification were made regarding a standard digital computer. However, Effector machines are expected to outperform standard parallel digital computers, because although the two sets of basic instructions can be performed in parallel, the basic instructions have a sequential nature to them. Additionally, even when a parallel computer can perform two instructions in parallel a relatively subtle and small programming error may result in the instructions not being performed in parallel. In contrast, the basic instructions of the Effector machines are parallel in nature and as disclosed have time as one of the parameters to help ensure parallel execution where ever parallel execution is specified. Further, by operating the transistors of the Effector machine at subthreshold, the total current used is lower and the total voltage/current swing is also lower. As a result of the total current being lower, the total resistive heat generates is lower. .

Thus, (1) the performance of the Effector machine advertised in the specification is reasonable as a result of the subtrheshold operation and the parallel nature of the Effecotrs, and (2) even if arguendo the statements about the performance were not true, (a) the invention is not entirely inoperative in that it still performs as a computing machine) even if not as fast as disclosed (which is adequate for satisfying 35 USC 112,

first paragraph) and (b) the performance is not claimed and 35 USC 112, first paragraph, only requires that the specification give an adequate written description of the claimed invention.

35 USC 112, second paragraph

Regarding claims 5, 6, 8, 11, 18, 27, 36, 48-58, the Office Action alleged that various that clauses were indefinite as a result of using the phrase "capable of" or equivalent phrases. Accordingly, claims have been amended to remove phrases including the word "capable," thereby obviating these grounds of rejection.

Regarding claim 6, the Office Action stated, "It is unclear if the 'machine of claim 5' in claim 6 refers to the system of claim 5," accordingly, claim 6 has been amended to recite, "The system of claim 5," thereby obviating this ground of rejection.

Regarding claim 8, the Office Action states, "It is unclear whether the output interpreter is part of the machine of claim 1 or if the output interpreter is external to the machine of claim 1." Regarding claim 14, the Office Action states, "It is unclear if it is necessary to actually possess the machine of claim 1 in order to use the method of claim 14. It appears that the method of claim 14 merely performs abstract graph manipulation and does not necessitate actually possessing the machine of claim 1." Also, regarding claims 8, 14, 47, and 48, the Office Action states, "It is unclear if the claimed system is the same as the machine of claim 1 or if the claimed system is not the same as the machine of claim 1.

MPEP 2173.05(f) states,

> A claim which makes reference to a preceding claim to define a limitation is an acceptable claim construction which should not necessarily be rejected as

> improper or confusing under 35 U.S.C. 112, second paragraph. For example, claims which read: "The product produced by the method of claim 1." or "A method of producing ethanol comprising contacting amylose with the culture of claim 1 under the following conditions ....." are not indefinite under 35 U.S.C. 112, second paragraph, merely because of the reference to another claim. See also *Ex parte Porter*, 25 USPQ2d 1144 (Bd. Pat. App. & Inter. 1992) where reference to "the nozzle of claim 7" in a method claim was held to comply with 35 U.S.C. 112, second paragraph.

In other words, according to MPEP 2173.05(f) it does not matter where in the claim a reference to a prior claim occurs. It also does not matter if the reference to the prior claim is for the method used or the item made by another method. Either way, the claim conforms with 35 USC 112, second paragraph. The Office Action has not given any reason why the current claim should be an exception, and the Applicant is not aware of anything in there is nothing in the present claim that would make them an exception to MPEP 2173.05(f). Specifically, contrary to the implications of the Office Action, the phrase "A system comprising... the machine of claim 1..." conforms with 35 USC 112, second paragraph; no differently than the phrase, "A system comprising... a machine...." Similarly, "A system comprising... an interpreter for designing the machine of claim 1..." conforms with 35 USC 112, second paragraph, no differently than "A system comprising... an interpreter for designing a machine...." When a system comprises a machine of claim 1, the machine of claim 1 is a component of the system. There is no confusion about if the system is the machine. Similarly, when a system comprises an interpreter that designs the machine of claim 1, there is no confusion about whether one has to be in possession of the machine of claim 1 just as there is no confusion about whether one needs to have possession of the nozzle of claim 7 in order to implement a method that makes the nozzle of claim 7.

Regarding claims 5, 14, 47, and 48 and the claims that depend from claims 5, 14, 47, and 48, the Office Action stated, "It is unclear if it is necessary to actually possess the invention" of an earlier claim 1 "in order to have the system" of a current claim because "any computer system should be capable of at least partially designing a computing machine" (the Office Action emphasized the phrase "at least partially"). Accordingly, the word partially has been deleted from claims 5, 14, 47, and 48, thereby obviating this ground of rejection.

Regarding claim 5, the Office Action states "It is unclear how the system of claim 5 would accomplish 'at least partially designing at least the machine of claim 1 ', if it were to actually be used to at least partially design such a machine." Regarding claim 47, "It is unclear how the system of claim 47 would accomplish 'at least partially designing at least a Static program for the machine of claim 1', if it were to actually be used to at least partially design at least such a program." The Office Action makes a similar statement about the Meta program of claim 48. As an aside, Section 6 (pages 8-13) of the specification explains that an evolution method, such as CGE can be used to design a Static program, Meta program and/or Effector machine, as an example of how to design a static, meta program, or effector machine. Specifically, an arbitrary set of static programs, meta programs, and/or effector machines are run and a subset of those programs are kept, where the subset are the static or meta programs that produce output parameters that give the closest match to the output parameters that correspond to each set of input parameters. The programs that are kept are varied (e.g., by mutation, crossing, and permutation). The new variations are run, and the best of the varied programs are kept. Then the process is repeated until a static or a meta program is found

that produces the appropriate output for a given training set of input. The assumption is that if the static program can produce the appropriate output for each training set and if there are enough training sets, the static program will also produce appropriate output for input that is not in the training set.

However, not claiming how to design an effector machine, a static program, or a meta program makes the claim generic to other methods of designing an effector machine, a static program, or a meta program, which makes the claims broad. In other words, not specifying "how" only makes the claim generic to any "how," but does not create any ambiguity as to the scope of the claim. MPEP 2173.04 states,

> **Breadth Is Not Indefiniteness**
>
> Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.

Since breadth is not indefiniteness, therefore there is no need for claims 5, 47 and 48 to recite "how," in contrast to the implications of the Office Action.

Regarding claim 8, the Office Action stated, "it is unclear how the interpreter would translate firing activity of a subset of Effectors, if it were to actually perform such a translation."

As an aside, the specification explains that the value at which an effector fires may be interpreted as different symbols or instructions. The specification also explains and alternative way of interpreting the firing in example 3.2 (at page 5), which states

> The sequence ($b0$; $b1$; $b2$; $b3$: : :) is a binary representation of a real number x in [0; 1]. If $bi = 1$, then choose Ei to fire at least once during the interval of time [0; γ]. If $bi = 0$, then choose Ei to not fire during the interval of time [0; γ].

Thus whether an effector fires or does not fire is interpreted as a one or a zero, and the output of a set of effectors represents binary data. It is old and well known to use binary data to represent other symbols and other data. Thus, one of ordinary skill in the art would know how to build an embodiment of the interpreter, based on the specification.

More importantly, under 35 USC 112, second paragraph, the claim does not need to specify a method or mechanism of how the interpreter performs the translating, because not stating how the translation is performed only makes the claim broader (by being generic to any method consistent with the rest of the claim), and breadth is not indefiniteness. The scope of the claim is clear - no matter how performed, as long as the translating is performed, the translating clause is met. Nonetheless, claim 8 is amended to recite, "translating firing activity of a subset of said Effectors into a desired output form" to clarify what is meant by "translating."

Regarding claims 11, 27, and 49, the Office Action states, "It is unclear what qualities and characteristics the machine would necessarily need to possess in order to run a Meta program, if it actually were used to run such a program." Again the lack of specification of "qualities" makes claims 11, 27, and 49 broad – not indefinite. Nonetheless, although not necessary, claims 11, 27, and 49, are amended via the above amendments to recite an input section and to recite the qualities of a Meta program in order to clarify what qualities and characteristics the machine has so that the machine can run the Meta program. Accordingly, the scope of claims 11, 27, and 49 is well defined, and via the above amendment the rejection of claims 11, 27 and 49 have been obviated.

Regarding claim 13, the Office Action states (referring to subthreshold operations), "It is unclear how the transistors are configured to operate in such a manner." However, the specification states (in the last paragraph before the claims, page 14),

> The schematic diagram titled Effector Circuit illustrates how one Effector can be implemented with a circuit built from transistors that operate subthreshold. .... In Carver Mead's words, for a transistor to operate subthreshold means: "The gate voltage at which the mobile charge [in the transistor] begins to limit the flow of current is called the threshold voltage....Most circuits described in this book operate in sub threshold–their gate voltage stay well below the threshold voltage," [MEAD]. Furthermore, when transistors operate subthreshold, the amount of heat produced is greatly reduced.

The citation for MEAD given in the specification and in the Information Discosure Statement is "[MEAD] Mead, Carver. (1989) Analog VLSI and Neural Systems. Addison Wesley Publishing Company. ISBN0201059924." In other words, the specification explains that a subthreshold circuit is one in which "the gate voltages of the transistors stay below their threshold voltage," where the threshold voltage is "the voltage at which the mobile charge in the transistor begins to limit the flow of current." Additionally, subthreshold circuits are explained in Mead and Carver's book, and consequently one of ordinary skill would understand what is meant operating transistors at, and circuits having transistors at, subthreshold. In other words, the application shows one example of a circuit for how to configure transistors to operate at subthreshold. Not claiming the circuit makes the claim generic to other subthreshold circuits, which makes the claims broad. The scope of the claim is clear – no matter how the subthreshold nature of the transistor is instilled within the claimed invention, as long as the transistor operates subthreshold, this clause of the claim is met. Stated differently, breadth is not indefiniteness, and therefore there is no need for claim 13 to recite "how." Nonetheless, although not necessary, claims 13 and 26 are amended to

recite the definition of subthreshold operation instead of relying on the specification for that definition.

Regarding claims 36, 38, 50 and 53, the Office Action questions whether the "distinct effector machine" was different than the earlier mentioned effector machine of independent claims 1 and 17. Accordingly, in claims 36, 38, and 50, the effector machine occurring in claim 1 is now labeled the first effector machine, and the word "distinct" is replaced with the word "second," thereby clarifying that it is a second effector machine.

35 USC 102

The Office Action rejected claims 1, 5, 17, 47 and 48 under 35 USC 102 as allegedly anticipated by Tomita.

The Office Action mentioned that calling computational elements Effectors does not make the claim patentable. The Applicant agrees, and has amended the claims to clarify that the computational elements will be referred to as Effectors, and consequently the terms "Effector" and "Effector machine" that appear in the claims are defined by the claim and are not defined by the definition in the specification.

Nonetheless, the Applicants disagree with the Office Action's allegation regarding Tomita being anticipitory. Tomita, column 5, lines 27-37, state

> Briefly described, the present invention provides a system (and method) for building an artificial neural network of artificial neurons on a computer using input data representing patterns of different classes of signals in which a programmed computer analyzes the input data to generate one or more data points in two or three dimensions representative of the signals in each of the different classes, and provides for visualizing the distribution of the data points on a map in two or three dimensions using an output device coupled to the computer.

In other words, in Tomita an ordinary digital computer is programmed to design a neural network. Thus, even assuming that (1) the neurons are the claimed computational elements and (2) determining the weights and connections between the neurons is the claimed determination of "how the Effectors behave" and "how information is transmitted from one Effector to another Effector," at best, in Tomita a digital computer is making this determination for a neural network that has not yet been built. In contrast, in Effector machine of claims 1, 5, 17, 47, and 48, the architecture of the Effector machine determines "how the Effectors [of the effector machine that architecture] behave" and the architecture the Effector machine "determines" how "information is transmitted from one Effector to another Effector" within the very same Effector machine having the architecture. In other words, the architecture that makes these determinations is part of the same Effector machine for which the determination is made and in contrast to Tomita is not the architecture of a completely different machine that is not even itself a neural network or Effector. This point is further emphasized in claims 1 and 17 by replacing the word "determines" with "adjusts" and inserting the phrase while running, thereby emphasizing that the architecture adjusts parameters of the Effectors while the machine is running.

Consequently, the Applicant respectfully submits that the digital program running an ordinary program written for a digital computer that designs the neural network of Tomita does not disclose, teach, or suggest the claimed Effector machine (whether a virtual or hardware effector machine) in which its own architecture determines or adjusts how its own Effectors behave and transmit data. Therefore, the Applicant respectfully submits that the rejection under 35 USC 102 is improper and should be withdrawn.

New Claims

New claim 59 recites converting firing activity into a series of symbols, which is useful for using the effector machine producing human readable output as may be useful for human readable programs and for other applications, such as a word processor, for example.

New claim 60 recites a virtual Effector machine stored as instructions on a machine readable medium, which has input as instructions native to an Effector machine and output as instructions native to the digital computer the virtual Effector machine runs on.

MPEP 2106.01(I) states,

> a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See *Lowry*, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, it is important to distinguish claims that define descriptive material *per se* from claims that define statutory inventions.

In other words, the computer-readable medium of claim 60 is a structural and functional element.

Prior to filing the present application, the virtual Java machine was known and was known to be used to allow the same JAVA program to run on multiple platforms and multiple physical machines. Similarly, a virtual Effector machine is an Effector machine written in a programming language, such as C or assembly language, inherently translates statements written in the language of the virtual Effector machine to a language understood by the machine on which the virtual Effector machine runs. This allows the

same Effector machine program to run on different platforms and different physical machines.

MPEP 2106.01(II) states,

> Nonfunctional descriptive material may be claimed in combination with other functional descriptive multi-media material on a computer-readable medium to provide the necessary functional and structural interrelationship to satisfy the requirements of 35 U.S.C. **101**. The presence of the claimed nonfunctional descriptive material is not necessarily determinative of nonstatutory subject matter. For example, ***a computer that recognizes a particular grouping or sequence of musical notes read from memory and thereafter causes another defined series of notes to be played, requires a functional interrelationship among that data and the computing processes performed when utilizing that data. As such, a claim to that computer is statutory subject matter*** because it implements a statutory process.<

The statutory process of converting one set of musical notes to another series of notes is analogous to converting one computer language to another computer language, as recited in claim 60, implying that claim 60 is statutory.

Additionally, *In re Toma*, 575 F.2d 872, 877, 197 USPQ 852, 856-57 (CCPA 1978), states,

> [T]he method for enabling a computer to translate natural languages is ... a method of operating a machine. The ... "useful" arts inquiry must focus on whether the claimed subject matter (a method of operating a machine to translate) is statutory, not on whether the product of the claimed subject matter (a translated text) is statutory, not on whether the prior art which the claimed subject matter purports to replace (translation by a human mind) is statutory, ... This was the law prior to Benson and was not changed by Benson.

Software for the translation from one computer language to another computer language (so that different machines can understand the same set of instructions) is analogous to software for translating one human language to another human language, which was determined to patentable under 35 USC 101 in *In re Toma* despite the decision in *Benson.* Therefore, claim 60, which translates the language of the virtual Effector machine to a

language understood by the underlying machine on which the virtual Effector machine runs is likewise patentable under 35 USC 101 according to *In re Toma.*

New claims 61 and 62 recite a hardware computing machine and a method for making a hardware computing machine in which time is one of the parameters of the effectors and therefore is distinguished from Tomita in addition to the reasons given above.

Conclusion

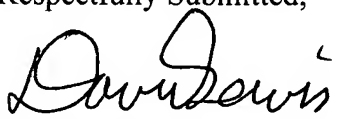
Therefore, for the above reasons, the Applicant respectfully submits that the present application is condition for allowance, and the Applicant respectfully requests that this application be allowed.

Please charge any fees that may be due (and that have not been paid for elsewhere) to Deposit Account # 503345.

An extension of time to the current date is hereby requested, if an extension of time is necessary. The fee for the extension of time may be billed to the above account number, if (1) there is not a check enclosed that already covers the extension of time, or (2) if a check was enclosed, but is insufficient to cover all of the fees due.

Please feel free to contact the Applicant's undersigned representative at 408-993-1800.

Respectfully Submitted,



David Lewis

July 20, 2007
Date

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